SECTION 12
ELECTRICAL AND THERMAL CHARACTERISTICS

The following paragraphs provide information on the maximum rating and thermal characteristics for the MC68060. This section is subject to change. For the most recent specifications, contact the AESOP electronic bulletin board at (800)843-3451 or (512)891-3650 (refer to **C.5.4 AESOP Electronic Bulletin Board** for connection information).

12.1 MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to 4.0	V
Input Voltage	V_{in}	–0.5 to V_{CC}+4	V
Maximum Operating Junction Temperature	T_J	110	°C
Minimum Operating Ambient Temperature	T_A	0	°C
Storage Temperature Range	T_{stg}	–55 to 150	°C

This device contains protective circuitry against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher that maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

12.2 THERMAL CHARACTERISTICS

Description	Symbol	Value	Unit
Thermal Resistance, Junction to Case—PGA	θ_{JC}	2.5	°C/W
Thermal Resistance, Junction to Case—CQFP	θ_{JC}	2.0	°C/W

12.3 POWER DISSIPATION

Conditions	MC68EC060			MC68LC060		MC68060		Unit
	40 MHz	50 MHz	66 MHz	50 MHz	66 MHz	50 MHz	66 MHz	
V_{cc} = 3.465 V, T_A = 0°C Normal Mode	3.1	3.5	4.5	3.5	4.5	3.9	4.9	W
V_{cc} = 3.465 V, T_A = 0°C LPSTOP Mode, CLK Running	300	300	300	300	300	300	300	mW
V_{cc} = 3.465 V, T_A = 0°C LPSTOP Mode, CLK Stopped Low	30	30	30	30	30	30	30	mW

NOTES:
1. Power dissipation values are preliminary and will likely be replaced with lower values upon further testing.
2. Power dissipation assumes no DC load.
3. Power dissipation figures are not applicable to the debug pipe control mode.

PRELIMINARY

12.4 DC ELECTRICAL SPECIFICATIONS (V_{CC} = 3.3 V_{DC} ± 5%)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2	5.5	V
Input Low Voltage	V_{IL}	GND	0.8	V
Undershoot	—	—	0.8	V
Overshoot	—	—	0.8	V
Input Leakage Current $\overline{AVEC}$, CLK, TT1, $\overline{BG}$, $\overline{CDIS}$, $\overline{MDIS}$, $\overline{IPLx}$, $\overline{RSTI}$, $\overline{SNOOP}$, $\overline{CLKEN}$, $\overline{TBI}$, $\overline{TCI}$, TCK, $\overline{TEA}$, $\overline{TA}$, $\overline{TRA}$, $\overline{BGR}$, $\overline{CLA}$, $\overline{JTAG}$	I_{IL}, I_{IH}	–50	20	µA
Hi-Z (Off-State) Leakage Current An, $\overline{BB}$, $\overline{CIOUT}$, Dn, $\overline{LOCK}$, $\overline{LOCKE}$, TDO, $\overline{TIP}$, $\overline{SAS}$, $\overline{BTT}$, $\overline{BSx}$, TMx, TLNx, $\overline{TS}$, TTx, UPAx	I_{TSI}	–50	20	µA
Signal Low Input Current, V_{IL} = 0.8 V TMS, TDI, $\overline{TRST}$	I_{IL}	–1.1	–0.18	mA
Signal High Input Current, V_{IH} = 2.0 V TMS, TDI, $\overline{TRST}$	I_{IH}	–0.94	–0.16	mA
Output High Voltage, I_{OH} = 16 mA	V_{OH}	2.4	—	V
Output Low Voltage, I_{OL} = 16 mA	V_{OL}	—	0.5	V
Capacitance*, V_{in} = 0 V, f = 1 MHz, CLK Only	C_{in}	—	20	pF
Capacitance*, V_{in} = 0 V, f = 1 MHz, All Inputs Except CLK	C_{in}	—	20	pF

*Capacitance is periodically sampled and not 100% tested.

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12.5 CLOCK INPUT SPECIFICATIONS (V_{CC} = 3.3 V_{DC} ± 5%)

Num	Characteristic	40 MHz[1]		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	
	Frequency of Operation	0[4]	40	0[4]	50	0[4]	66.67	MHz
1	CLK Cycle Time	25	—	20	—	15	—	ns
2	CLK Rise Time	—	2	—	2	—	2	ns
3	CLK Fall Time	—	2	—	2	—	2	ns
4	CLK Duty Cycle Measured at 1.5 V	45	55	45	55	45	55	%
4a[2]	CLK Pulse Width High Measured at 1.5 V	11.25	13.75	9	11	6.75	8.25	ns
4b[2]	CLK Pulse Width Low Measured at 1.5 V	11.25	13.75	9	11	6.75	8.25	ns
55	$\overline{\text{CLKEN}}$ Input Setup	8	—	7	—	5	—	ns
56	$\overline{\text{CLKEN}}$ Input Hold	2	—	2	—	2	—	ns

NOTES:
1. 40 MHz available only for the MC68EC060.
2. Specification value at maximum frequency of operation.
3. CLK may be stopped LOW to conserve power.
4. Minimum frequency is periodically sampled and not 100% tested.

PRELIMINARY

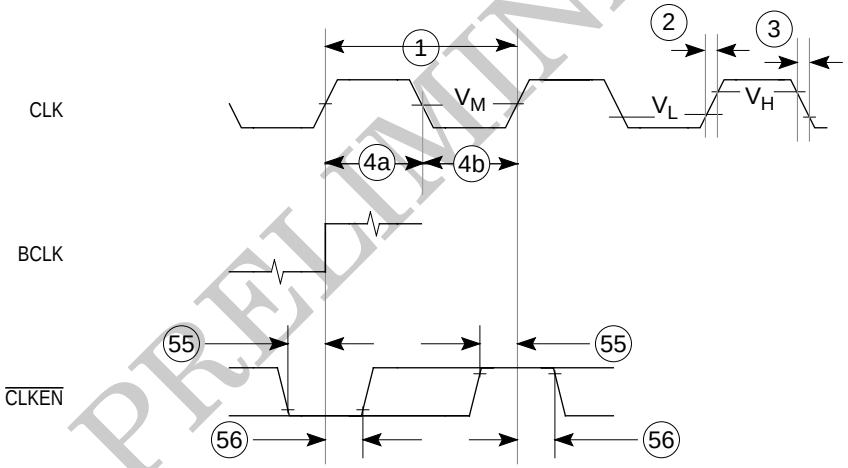


Figure 12-1. Clock Input Timing Diagram

12.6 OUTPUT AC TIMING SPECIFICATIONS (V_{CC} = 3.3 V_{DC} ± 5%)

Num	Characteristic	40 MHz[1]				50 MHz				66 MHz				Unit
		Pad Starts at 5.5 V[3]		Pad Starts at V_{CC} [3]		Pad Starts at 5.5 V [3]		Pad Starts at V_{CC}[3]		Pad Starts at 5.5 V [3]		Pad Starts at V_{CC} [3]		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
11[5]	BCLK to Address CIOUT, LOCK, LOCKE, R/W, SIZx, TLN, TMx, TTx, UPAx, BSx Valid (signal pre-driven)	—	—	3	17	—	—	3	12.6	—	—	3	9.9	ns
11a[5]	BCLK to Address CIOUT, LOCK, LOCKE, R/W, SIZx, TLN, TMx, TTx, UPAx, BSx Valid (Signal from three-state)	3	19	3	18	3	15.4	3	13.5	3	11.8	3	10.4	ns
12	BCLK or CLK to Output Invalid (Output Hold)	3	–	3	–	3	–	3	–	3	–	3	–	ns
13	BCLK to TS Valid	3	19	3	18	3	14.4	3	12.3	3	10.9	3	9.5	ns
14	BCLK to TIP Valid	3	19	3	18	3	15.4	3	13.5	3	11.8	3	10.4	ns
18	BCLK to Data Out Valid	3	19	3	18	3	13.5	3	13.5	3	10.4	3	10.4	ns
19	BCLK to Data Out Invalid (Output Hold)	3	–	3	–	3	–	3	–	3	–	3	–	ns
21	BCLK to Data-Out High Impedance	—	15	—	15	—	12	—	12	—	10	—	10	ns
38	BCLK to Address, CIOUT, LOCK, LOCKE, R/W, SIZx, TS, TLNx, TMx, TTx, UPAx, BSx High Impedance	—	15	—	15	—	12	—	12	—	10	—	10	ns
39	CLK to BB, TIP High Impedance	—	15	—	15	—	12	—	12	—	10	—	10	ns
40[5]	BCLK to BR, BB Valid (Signal Pre-driven)	—	—	3	17	—	—	3	12.6	—	—	3	9.9	ns
40a[5]	BCLK to BB Valid (signal from three-state)	3	19	3	18	3	15.4	3	13.5	3	11.8	3	10.4	ns
50[6]	CLK to IPEND, PSTx, RSTO Valid	—	—	3	18	—	—	3	13.5	—	—	3	10.4	ns
57	BCLK to SAS Valid	3	19	3	18	3	15.4	3	13.5	3	11.8	3	10.4	ns
58	BCLK to SAS Invalid (Output Hold)	3	–	3	–	3	–	3	–	3	–	3	–	ns
59	BCLK to SAS High Impedance	—	15	—	15	—	12	—	12	—	10	—	10	ns
60	BCLK to TS Invalid (Output Hold)	3	–	3	–	3	–	3	–	3	–	3	–	ns
61	BCLK to BTT Valid	3	19	3	18	3	15.4	3	13.5	3	11.8	3	10.4	ns
62	BCLK to BTT Invalid (Output Hold)	3	–	3	–	3	–	3	–	3	–	3	–	ns
63	BCLK to BTT High Impedance	—	15	—	15	—	12	—	12	—	10	—	10	ns

PRELIMINARY

NOTES:
1. 40 MHz available only for the MC68EC060.
2. Output timing is measured at the pin. The specifications assume a capacitive load of 50 pF. However, a maximum load of 130 pF may be used at each pin. Characterization data shows that at 130 pF loads, output propagation delays are as follows: 40 MHz, Pad at V_{CC}, multiply by prop delay by 1.4; 40 MHz, Pad at 5.5, multiply prop delay by 1.6; 50 MHz, Pad at V_{CC}, multiply prop delay by 1.4; 50 MHz, Pad at 5.5, multiply prop delay by 1.6; 66 MHz, Pad at V_{CC}, multiply prop delay by 1.3; 66 MHz, pad at 5.5, multiply prop delay by 1.4. Exceeding the 130-pF limit on any pin might affect long-term reliability and Motorola does not guarantee proper operation.
3. When interfacing the processor to a system designed for 5-volt operation, the “Pad Starts at 5.5” column must be used when it is possible that the pin is at 5.5 volts when the processor begins to drive. Once a pin is driven by the processor and is not three-stated, the “Pad Starts at Vcc” column may be used. If the processor is in a system designed for 3.3-volt operation, use the “Pad Starts at Vcc” column always. This note not applicable to specs 11,11a, 40, and 40a. Refer to note 5 for these specs.
4. BCLK is not a pin signal name. It is a virtual bus clock derived from the combination of CLK and CLKEN. A BCLK rising edge coincides with a CLK in which CLKEN is asserted. A BCLK falling edge is insignificant. When a reference to BCLK is used to describe output timing, it means that the specific output transitions only on rising CLK edges in which CLKEN is asserted. A timing reference to CLK means that the output may transition off the rising CLK edge, including those rising edges in which CLKEN is negated.
5. When the processor drives these signals from a three-stated condition, use spec 11a or 40a. Use the “Pad Starts at

V_{CC}" column or "Pad Starts at 5.5" column as applicable. Once these signals are driven, subsequent transitions are defined by spec 11 or 40. The "Pad Starts at 5.5" column is deleted from specs 11 and 40 since the processor drives up to the V_{CC} level only. $\overline{BR}$ is never three-stated by the processor, and therefore, spec 40a does not apply for $\overline{BR}$.

6.)"Pad Starts at 5.5" does not apply since these signals are always driven.

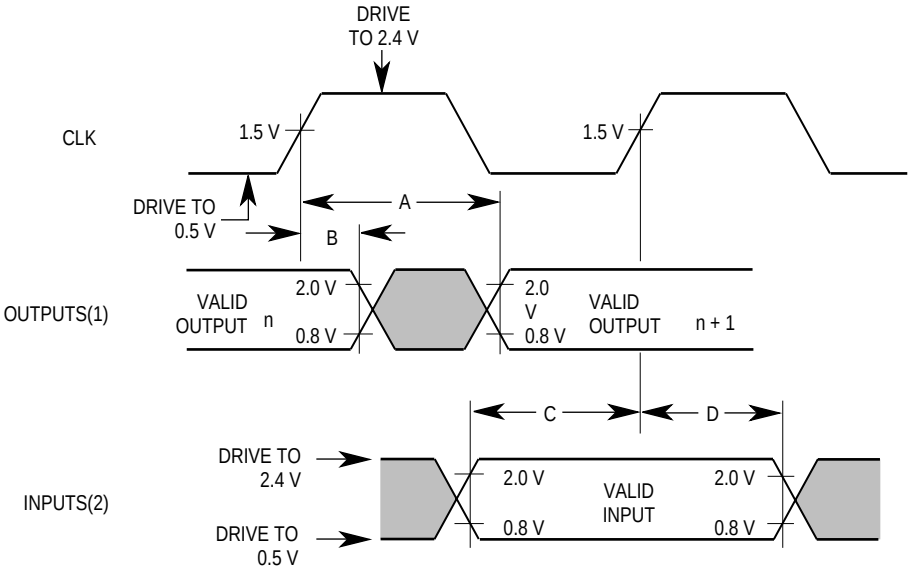
PRELIMINARY

12.7 INPUT AC TIMING SPECIFICATIONS (V_{CC} = 3.3 V_{DC} ± 5%)

Num	Characteristic	40 MHz[2]		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min.	Max.	
15	Data-In Valid to BCLK (Setup)	3	—	2	—	1	—	ns
16	BCLK to Data-In Invalid (Hold)	2	—	2	—	2	—	ns
17	BCLK to Data-In High Impedance (Read Followed by Write)	—	7	—	7	—	7	ns
22a	$\overline{TA}$, Valid to BCLK (Setup)	12	—	10	—	7	—	ns
22b	$\overline{TEA}$ Valid to BCLK (Setup)	12	—	10	—	7	—	ns
22c	$\overline{TCI}$ Valid to BCLK (Setup)	12	—	10	—	7	—	ns
22d	$\overline{TBI}$ Valid to BCLK (Setup)	12	—	10	—	7	—	ns
22e	$\overline{TRA}$ Valid to BCLK (Setup)	12	—	10	—	7	—	ns
23	BCLK to $\overline{TA}$, $\overline{TEA}$, $\overline{TCI}$, $\overline{TBI}$, $\overline{TRA}$ Invalid (Hold)	2	—	2	—	2	—	ns
24	$\overline{AVEC}$ Valid to BCLK (Setup)	12	—	10	—	7	—	ns
25	BCLK to $\overline{AVEC}$ Invalid (Hold)	2	—	2	—	2	—	ns
41a	$\overline{BB}$ Valid to BCLK (Setup)	12	—	10	—	7	—	ns
41b	$\overline{BG}$ Valid to BCLK (Setup)	12	—	10	—	7	—	ns
41c	$\overline{CDIS}$, $\overline{MDIS}$ Valid to BCLK (Setup)	12	—	10	—	7	—	ns
41d	$\overline{IPL}$≈ Valid to CLK (Setup)	3	—	2	—	1	—	ns
41e	$\overline{BTT}$ Valid to BCLK (Setup)	12	—	10	—	7	—	ns
41f	$\overline{BGR}$ Valid to BCLK (Setup)	12	—	10	—	7	—	ns
42a	BCLK to $\overline{BB}$ Invalid (Hold)	2	—	2	—	2	—	ns
42b	BCLK to $\overline{BG}$ Invalid (Hold)	2	—	2	—	2	—	ns
42c	BCLK to $\overline{CDIS}$, $\overline{MDIS}$ Invalid (Hold)	2	—	2	—	2	—	ns
42d	CLK to $\overline{IPL}$x Invalid (Hold)	2	—	2	—	2	—	ns
42e	BCLK to $\overline{BTT}$ Invalid (Hold)	2	—	2	—	2	—	ns
42f	BCLK to $\overline{BGR}$ Invalid (Hold)	2	—	2	—	2	—	ns
44a	Address Valid to BCLK (Setup)	3	—	2	—	1	—	ns
44c	TT1 Valid to BCLK (Setup)	12	—	10	—	7	—	ns
44e	$\overline{SNOOP}$ Valid to BCLK (Setup)	12	—	10	—	7	—	ns
45a	BCLK to Address Invalid (Hold)	2	—	2	—	2	—	ns
45c	BCLK to TT1 Invalid (Hold)	2	—	2	—	2	—	ns
45e	BCLK to $\overline{SNOOP}$ Invalid (Hold)	2	—	2	—	2	—	ns
46	$\overline{TS}$ Valid to BCLK (Setup)	12	—	10	—	7	—	ns
47	BCLK to $\overline{TS}$ Invalid (Hold)	2	—	2	—	2	—	ns
49	BCLK to $\overline{BB}$ in High Impedance (MC68060 Assumes Bus Mastership)	—	3	—	3	—	3	ns
51	$\overline{RSTI}$ Valid to BCLK	3	—	2	—	1	—	ns
52	BCLK to $\overline{RSTI}$ Invalid (hold)	2	—	2	—	2	—	ns
53	Mode Select Setup to BCLK ($\overline{RSTI}$ Asserted)	12	—	10	—	7	—	ns
54	BCLK to Mode Selects Invalid ($\overline{RSTI}$ Asserted)	2	—	2	—	2	—	ns
64	$\overline{CLA}$ Valid to BCLK (Setup)	12	—	10	—	7	—	ns
65	BCLK to $\overline{CLA}$ Invalid (Hold)	2	—	2	—	2	—	ns

NOTES:
1. BCLK is not a pin signal name. It is a virtual bus clock derived from the combination of CLK and $\overline{CLKEN}$. A BCLK rising edge coincides with a CLK in which $\overline{CLKEN}$ is asserted. A BCLK falling edge is insignificant. When a reference to BCLK is used to describe input timing, it means that the specific input is recognized only on rising CLK edges in which $\overline{CLKEN}$ is asserted. A timing reference to CLK means that the input is recognized at any rising CLK edge, including those edges in which $\overline{CLKEN}$ is negated.
2. 40 MHz available only for the MC68EC060.

PRELIMINARY



NOTES:

1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This input timing is applicable to all parameters specified relative to the rising edge of the clock.

LEGEND:

A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.

Figure 12-2. Drive Levels and Test Points for AC Specifications

PRELI

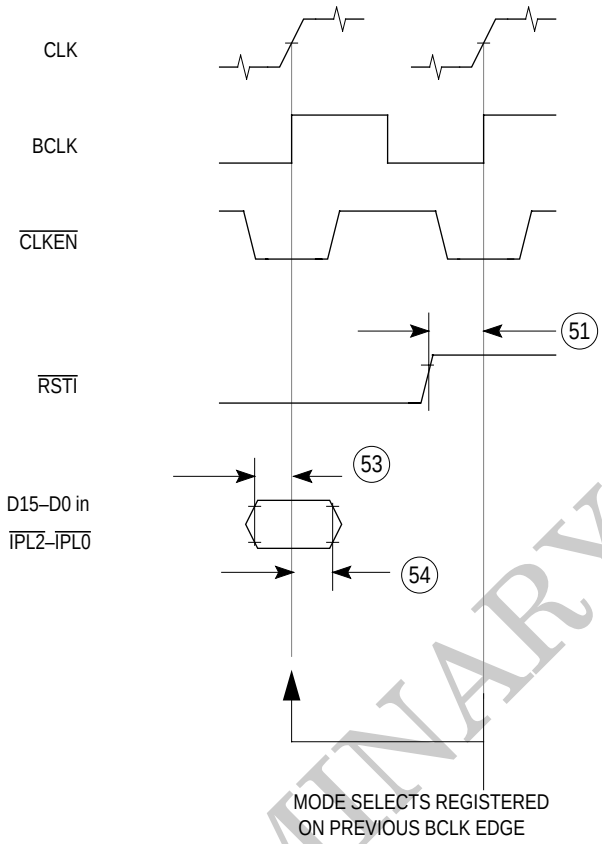
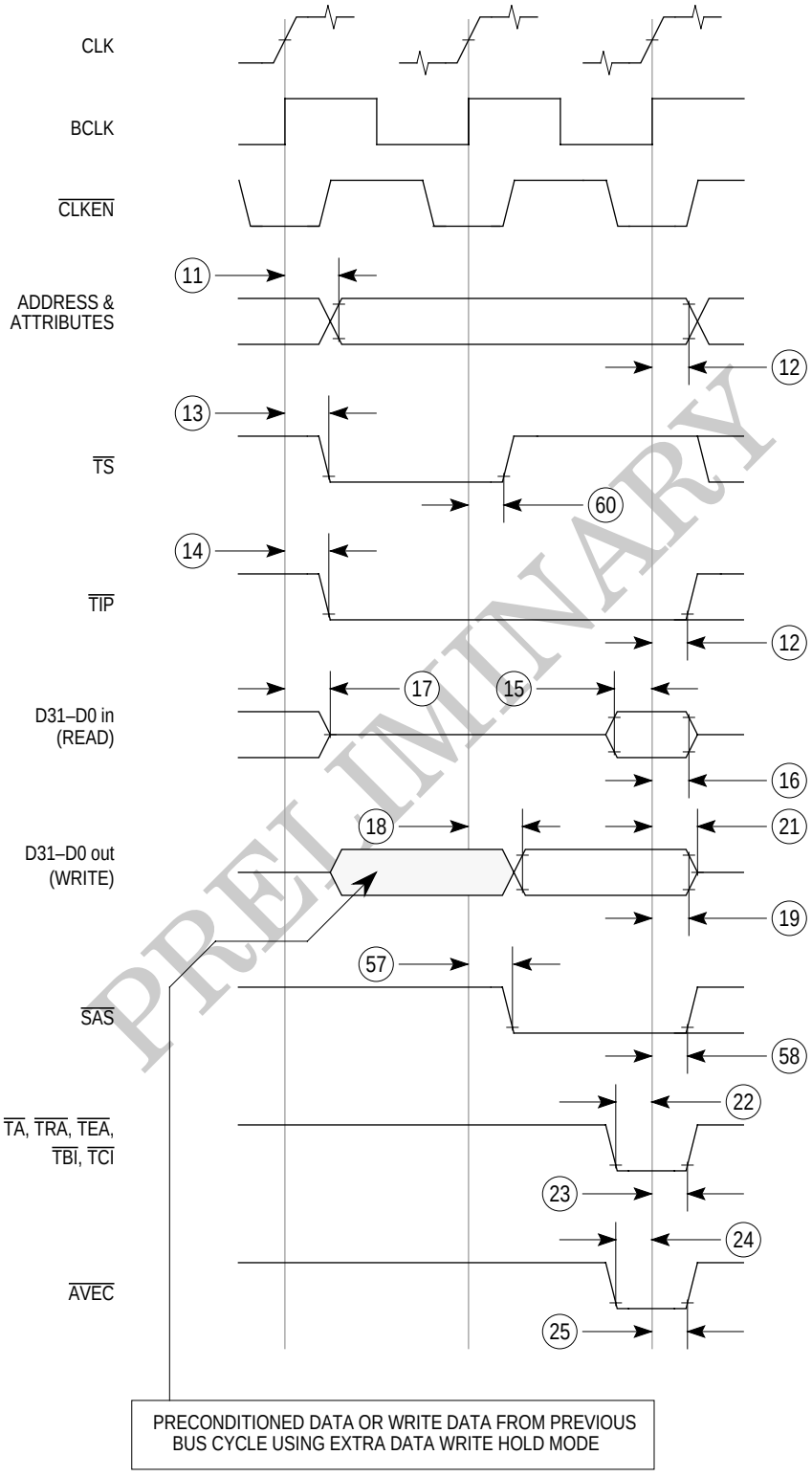


Figure 12-3. Reset Configuration Timing

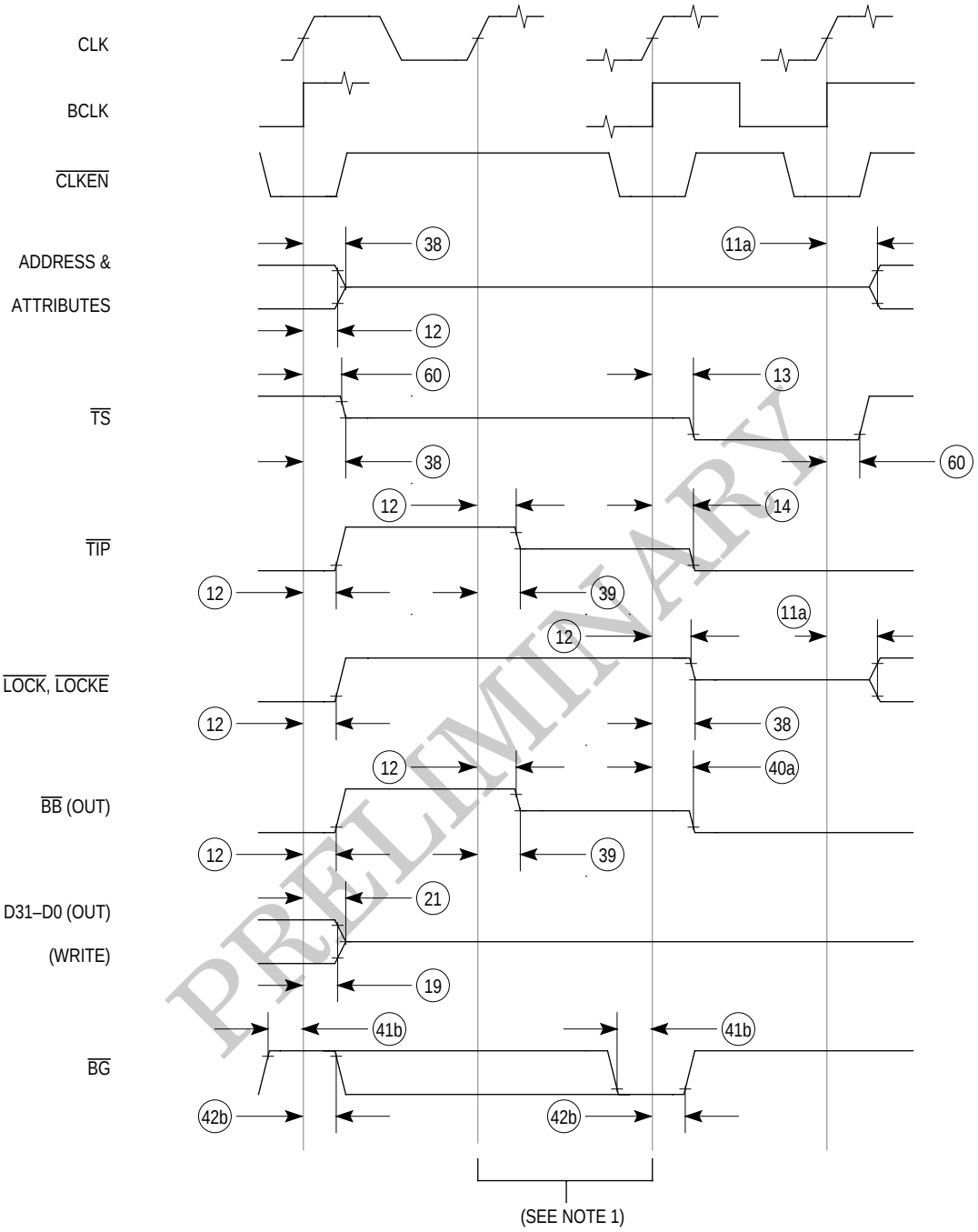
PRELIMINARY



PRELIMINARY

NOTE: Address and attributes refer to the following signals:
A31–A0, SIZ1, SIZ0, R/$\overline{W}$, TT1, TT0, TM2–TM0, TLN1, TLN0, UPA1, UPA0, $\overline{CIOUT}$, $\overline{BS3}$–$\overline{BS0}$

Figure 12-4. Read/Write Timing

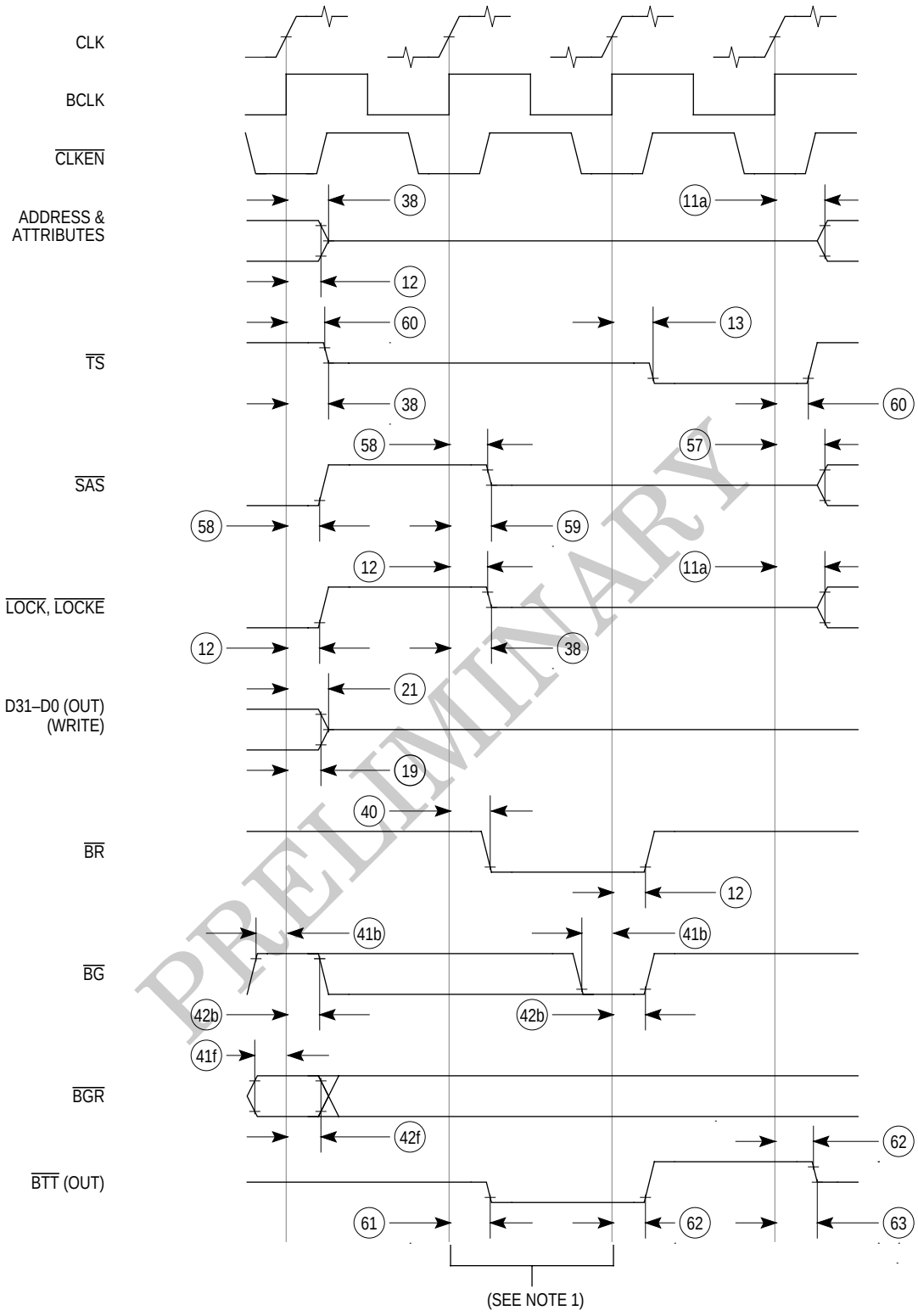


PRELIMINARY

NOTES:

1. For illustrative purposes, a bus mastership hand-over is shown after a locked bus cycle sequence which adds one extra clock period between the bus mastership hand-over that would not occur for a bus mastership hand-over after a non-locked bus cycle.
2. Address and attributes refer to the following signals:
   A31–A0, SIZ1, SIZ0, R/$\overline{W}$, TT1, TT0, TM2–TM0, TLN1, TLN0, UPA1, UPA0, $\overline{CIOUT}$, $\overline{BS3}$–$\overline{BS0}$

Figure 12-5. Bus Arbitration Timing

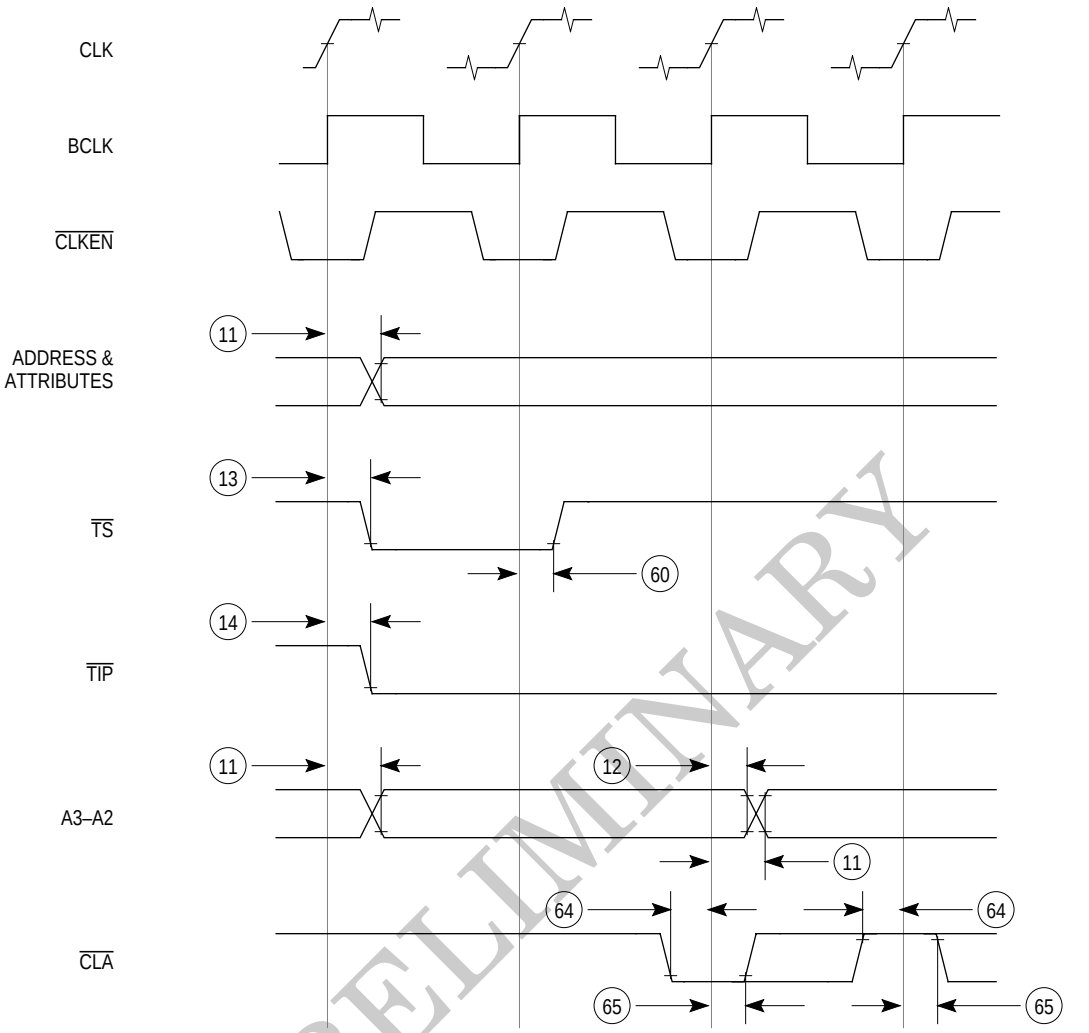


PRELIMINARY

NOTES:

1. For illustrative purposes, a bus mastership hand-over is shown after a locked bus cycle sequence which adds one extra clock period between the bus mastership hand-over that would not occur for a bus mastership hand-over after a non-locked bus cycle.
2. Address and attributes refer to the following signals:
   A31–A0, SIZ1, SIZ0, R/$\overline{W}$, TT1, TT0, TM2–TM0, TLN1, TLN0, UPA1, UPA0, $\overline{CIOUT}$, $\overline{BS3}$–$\overline{BS0}$

Figure 12-6. Bus Arbitration Timing (Continued)



NOTE: Address and attributes refer to the following signals: A31–A0, SIZ1, SIZ0, R/$\overline{W}$, TT1, TT0, TM2–TM0, TLN1, TLN0, UPA1, UPA0

Figure 12-7. $\overline{CLA}$ Timing

PRELIMINARY

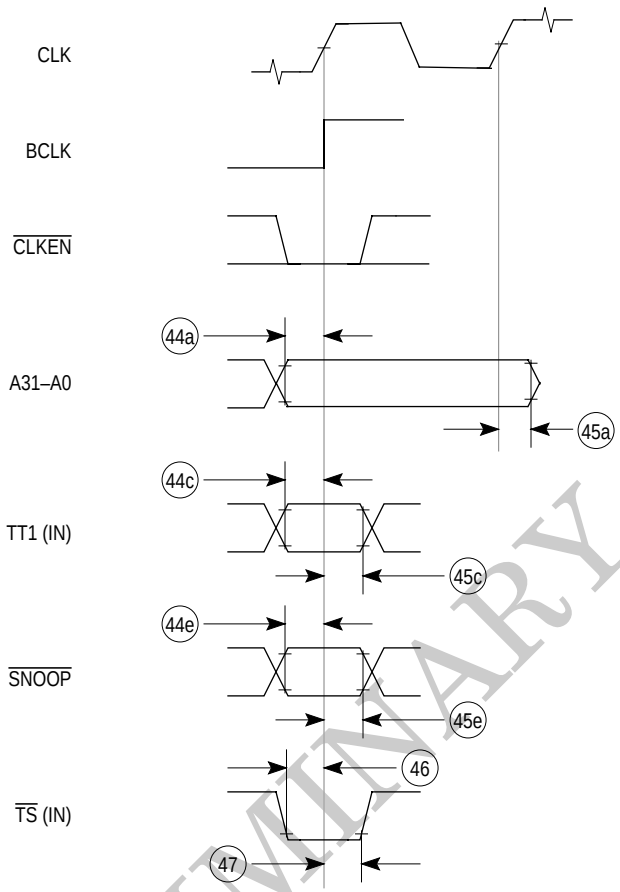
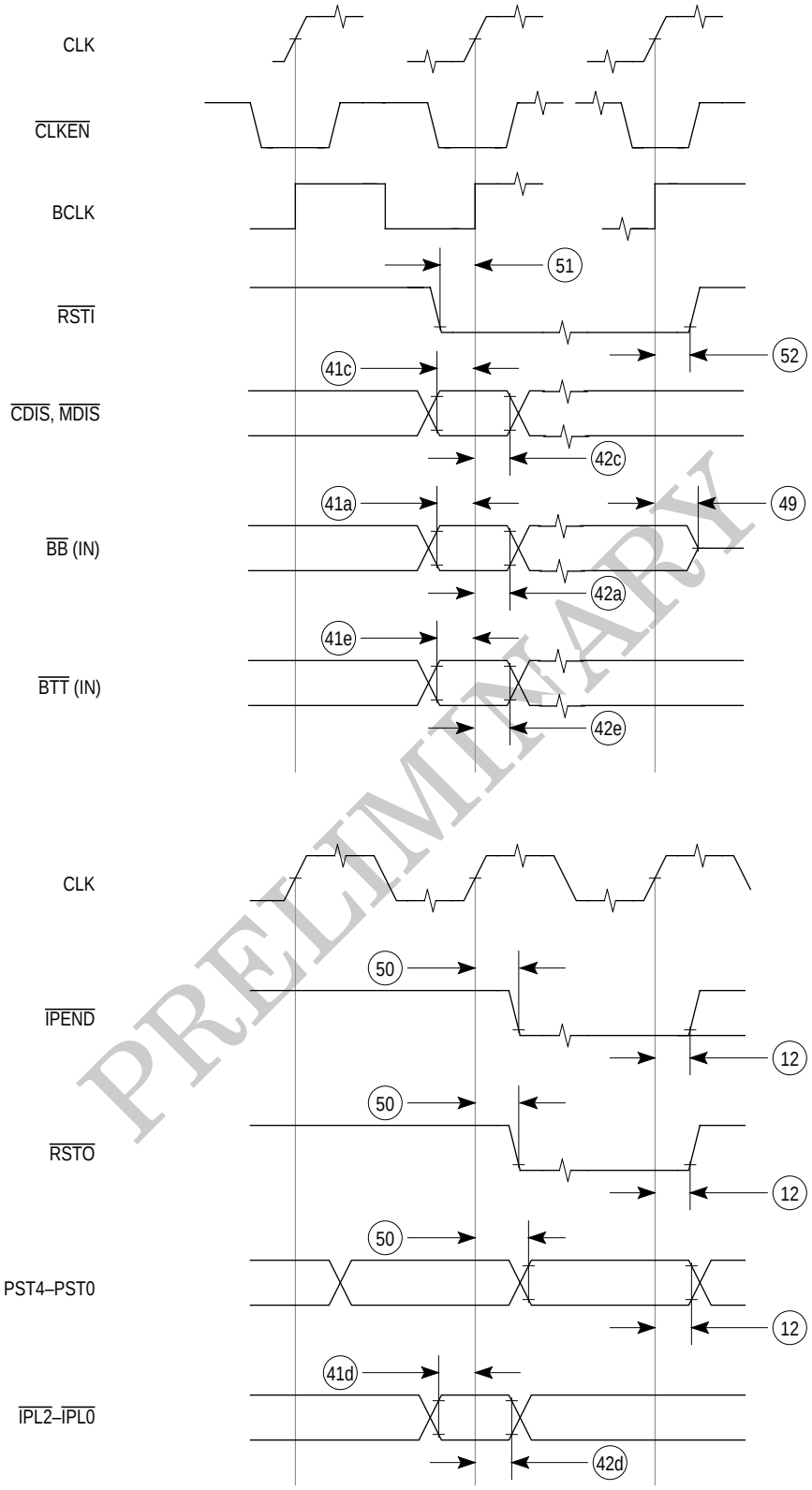


Figure 12-8. Snoop Timing

PRELIMINARY



PRELIMINARY

Figure 12-9. Other Signals Timing